

UCD30xx Memory Controller (MMC) Programmer's Manual

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1 Memory Controller - MMC

All MMC control Registers have the following attributes:

- 16-bit wide
- Addresses placed on word boundaries
- 16-bit data is placed on the least significant data bus D[15:0]
- Only half-word writes are permitted
- Registers are readable in any mode, but writeable only in privilege mode

1.1 Static Memory Control Register (SMCTRL)

Address **FFFFFD00**

Bit Number	13:12	11:9	7:4	3	1:0
Bit Name	LEAD	TRAIL	ACTIVE	ENDIAN	WIDTH
Access	R/W	R/W	R/W	R	R/W
Default	00	000	0000	-	00

Bits 13-12: LEAD – Address setup time cycles (write operations)

- 00 = No setup time required (Default)
- 01 = Write strobe is delayed one cycle
- 10 = Write strobe is delayed two cycles
- 11 = Write strobe is delayed three cycles

Bits 11-9: TRAIL – Number of Trailing wait states. Determine the trailing wait states after read and write operations to the memory associated with the chip select corresponding to the wait states.

Bit s 7-4: ACTIVE – Active Wait states (both read/write operations)

- 0000 = 0 Wait states (Default)
- 0001 = 1 Wait states
- 0010 = 2 Wait states
- 0011 = 3 Wait states
- 0100 = 4 Wait states
- 0101 = 5 Wait states
- 0110 = 6 Wait states
- 0111 = 7 Wait states
- 1000 = 8 Wait states
- 1001 = 9 Wait states
- 1010 = 10 Wait states
- 1011 = 11 Wait states
- 1100 = 12 Wait states
- 1101 = 13 Wait states
- 1110 = 14 Wait states
- 1111 = 15 Wait states

Bit 3: ENDIAN – Endian Mode Identification

- 0 = CPU configured in big endian mode

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1 = CPU configured in little endian mode

Bits 1-0: WIDTH – Data Width for Memories

00 = 8 bits (Default)

01 = 16 bits

10 = 32 bits

11 = Reserved

1.2 Write Control Register (WCTRL)

Address FFFFD2C

Bit Number	1	0
Bit Name	TRAIL_OVR	WBUF_ENA
Access	R/W	R/W
Default	0	0

Bit 1: TRAIL_OVR – Write trailing wait state override.

0 = At least one trailing wait state (Default)

1 = TRAIL bits (Bits 11-9 of SMCTRL register) sets trailing wait states

Bit 0: WBUF_ENA – Write buffer enable. When this bit is 1, the memory controller latches the data and control signals in the first cycle for write operations to the memories and peripherals on the expansion bus and lets the CPU perform other operations. However, the CPU starts a wait state if there is another request before the memory controller finishes.

0 = Write buffer disabled (Disabled)

1 = Write buffer enabled

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1.3 Peripheral Control Register (PCTRL)

Address FFFFD30

Bit Number	4:1	0
Bit Name	CLK_DIV	PBUF_ENA
Access	R/W	R/W
Default	1111	0

Bits 4-1: CLK_DIV – Peripheral clock divided ratio. Determine the division ratio for ICLK with respect to SYSCLK.

0000 = ICLK = SYSCLK

0001 = ICLK = SYSCLK/2

0010 = ICLK = SYSCLK/3

0011 = ICLK = SYSCLK/4

0100 = ICLK = SYSCLK/5

0101 = ICLK = SYSCLK/6

0110 = ICLK = SYSCLK/7

0111 = ICLK = SYSCLK/8

1000 = ICLK = SYSCLK/9

Deleted: 4

Deleted: 5

Deleted: 6

Deleted: 7

Deleted: 8

Deleted: 9

1001 = ICLK = SYSCLK/10

1010 = ICLK = SYSCLK/11

1011 = ICLK = SYSCLK/12

1100 = ICLK = SYSCLK/13

1101 = ICLK = SYSCLK/14

1110 = ICLK = SYSCLK/15

1111 = ICLK = SYSCLK/16 (Default at reset)

Deleted: 10

Deleted: 11

Deleted: 12

Deleted: 13

Deleted: 14

Deleted: 15

Bit 0: PBUF_ENA – Write buffer enable. When this bit is set to 1, the memory controller latches the data and control signals in the first cycle for write operations to the memories and peripherals on the expansion bus and lets the CPU perform other operations. However, the CPU starts a wait state if there is another request before the memory controller finishes.

0 = Write buffer disabled (Default)

1 = Write buffer enabled

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1.4 Peripheral Location Register (PLOC)

Address FFFFD34

Bit Number	15:0
Bit Name	LOC
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: LOC – These 16 bits represent the peripheral location bits, which correspond to each of the 16 peripheral selects.

0 = Peripheral is internal (Default)

1 = Peripheral is external

For example:

Bit 1 = 0 implies Peripheral Select[1] is internal.

Bit 1 = 1 implies Peripheral Select[1] is external.

Bit 8 = 0 implies Peripheral Select[8] is internal.

Bit 8 = 1 implies Peripheral Select[8] is external.

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1.5 Peripheral Protection Register (PPROT)

Address FFFFD38

Bit Number	15:0
Bit Name	PROT
Access	R/W
Default	0000_0000_0000_0000

Bits 15-0: PROT – These 16 bits represent the peripheral protection bits, which correspond to each of the 16 peripheral selects.

0 = Peripheral is accessible in all modes (Default)

1 = Peripheral is accessible in privilege mode only

For example:

Bit 0 = 0 implies Peripheral Select[0] is accessible in all modes.

Bit 0 = 1 implies Peripheral Select[0] is accessible in privilege mode only.

Bit 5 = 0 implies Peripheral Select[5] is accessible in all modes.

Bit 5 = 1 implies Peripheral Select[5] is accessible in privilege mode only.

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